CLAIMS

We claim:

1. Circuitry comprising a first differential transistor pair (e.g., M6, M7) connected between a first load device (e.g., M4) and a first current sink (e.g., **102**), wherein:

a first inductance-creating element (e.g., M2) is connected to the first load device to add inductance at a first output node (e.g., VON) of the circuitry; and

a power-supply rejection element (e.g., M1 and I1) is connected between the first inductance-creating element and a first voltage reference (e.g., VDD) to provide power-supply rejection at the first output node.

2. The invention of claim 1, further comprising:

a second load device (e.g., M5) connected to the first differential transistor pair; and

a second inductance-creating element (e.g., M3) connected to the second load device to add inductance at a second output node (e.g., VOP) of the circuitry, wherein the power-supply rejection element is connected between the second inductance-creating element and the first voltage reference to provide power-supply rejection at the second output node.

3. The invention of claim 2, further comprising a second differential transistor pair (e.g., M8, M9 of Fig. 2) connected between the first and second load devices and a second current sink (e.g., **104**) such that the circuitry is adapted to provide a variable-gain amplifier (VGA) function.

4. The invention of claim 3, wherein, when current through the first current sink increases, current through the second current sink is adapted to decrease such that total current through the first and second current sinks remains substantially constant to provide the VGA function with near exponential gain control.

5. The invention of claim 3, further comprising:

a common-mode sense circuit (e.g., **206**) connected to the first and second output nodes and adapted to generate a sensed common-mode voltage signal (e.g., **208**); and

a differential amplifier (e.g., **207**) connected to receive the sensed common-mode voltage signal and a desired common mode voltage signal (e.g., Vcmref) and adapted to generate and apply a common-mode error-correction signal to the first and second inductance-creating elements to correct for differences between the sensed and the desired common-mode voltage signals.

6. The invention of claim 5, further comprising:

a first capacitor (e.g., CL1 of Fig. 3) connected between the first output node and a second reference voltage (e.g., VSS); and

a second capacitor (e.g., CL2) connected between the second output node and the second reference voltage such that the circuitry is adapted to provide a continuous-time filter (CTF) function in addition to the VGA function.

7. The invention of claim 6, wherein the first and second capacitors are variable capacitors.

8. The invention of claim 6, wherein the power-supply rejection element comprises a current source (e.g., I1) whose current is controlled by a control signal that is adapted to be adjusted to adjust equivalent resistance provided by the first and second inductance-creating elements.

9. The invention of claim 2, further comprising:

a common-mode sense circuit (e.g., **206**) connected to the first and second output nodes and adapted to generate a sensed common-mode voltage signal (e.g., **208**); and

a differential amplifier (e.g., **207**) connected to receive the sensed common-mode voltage signal and a desired common mode voltage signal (e.g., Vcmref) and adapted to generate and apply a common-mode error-correction signal to the first and second inductance-creating elements to correct for differences between the sensed and the desired common-mode voltage signals.

10. The invention of claim 9, further comprising:

a first capacitor (e.g., CL1 of Fig. 4) connected between the first output node and a second reference voltage; and

a second capacitor (e.g., CL2) connected between the second output node and the second reference voltage such that the circuitry is adapted to provide a continuous-time filter (CTF) function.

11. The invention of claim 10, wherein the first and second capacitors are variable capacitors.

12. The invention of claim 10, wherein the power-supply rejection element comprises a current source (e.g., I1) whose current is controlled by a control signal that is adapted to be adjusted to adjust equivalent resistance provided by the first and second inductance-creating elements.

13. The invention of claim 1, further comprising:

a second load device (e.g., M5 of Fig. 2) connected to the first differential transistor pair;

a second inductance-creating element (e.g., M3) connected to the second load device to add inductance at a second output node (e.g., VOP) of the circuitry, wherein the power-supply rejection element is connected between the second inductance-creating element and the first voltage reference to provide power-supply rejection at the second output node;

a second differential transistor pair (e.g., M8, M9) connected between the first and second load devices and a second current sink (e.g., **104**) such that the circuitry is adapted to provide a variable-gain amplifier (VGA) function;

a common-mode sense circuit (e.g., **206**) connected to the first and second output nodes and adapted to generate a sensed common-mode voltage signal (e.g., **208**); and

a differential amplifier (e.g., **207**) connected to receive the sensed common-mode voltage signal and a desired common mode voltage signal (e.g., Vcmref) and adapted to generate and apply a common-mode error-correction signal to the first and second inductance-creating elements to correct for differences between the sensed and the desired common-mode voltage signals, wherein:

the first differential transistor pair comprises transistor M6 and transistor M7;

the second differential transistor pair comprises transistor M8 and transistor M9;

the first load device comprises transistor M4;

the second load device comprises transistor M5;

the first inductance-creating element comprises transistor M2;

the second inductance-creating element comprises transistor M3;

the power-supply rejection element comprises transistor M1 and current source I1;

a first input node VIP is connected to the gates of transistors M6 and M9;

a second input node VIN is connected to the gates of transistors M7 and M8;

the sources of transistors M6 and M7 are connected to the first current sink;

the sources of transistors M8 and M9 are connected to the second current sink;

the drains of transistors M6 and M8 are connected to the first output node VON and to the source of transistor M4;

the drains of transistors M7 and M9 are connected to the second output node VON and to the source of transistor M5;

the drains of transistors M4 and M5 are connected to the first reference voltage VDD;

the gate of transistor M4 is connected to the drain of transistor M2;

the gate of transistor M5 is connected to the drain of transistor M3;

the sources of transistors M1, M2, and M3 are connected together and to receive the common-mode error-correction signal; and

the gates of transistors M1, M2, and M3 and the drain of transistor M1 are connected together and to receive the current from current source I1.

14. The invention of claim 13, wherein, when current through the first current sink increases, current through the second current sink is adapted to decrease such that total current through the first and second current sinks remains substantially constant to provide the VGA function with near exponential gain control.

15. The invention of claim 13, further comprising:

a first variable capacitor (e.g., CL1 of Fig. 3) connected between the first output node and a second reference voltage; and

a second variable capacitor (e.g., CL2) connected between the second output node and the second reference voltage such that the circuitry is adapted to provide a continuous-time filter (CTF) function in addition to the VGA function.

16. The invention of claim 15, wherein the current of current source I1 is controlled by a control signal that is adapted to be adjusted to adjust equivalent resistance provided by transistors M2 and M3.

17. The invention of claim 1, further comprising:

a second load device (e.g., M5 of Fig. 4) connected to the first differential transistor pair;

a second inductance-creating element (e.g., M3) connected to the second load device to add inductance at a second output node (e.g., VOP) of the circuitry, wherein the power-supply rejection element is connected between the second inductance-creating element and the first voltage reference to provide power-supply rejection at the second output node;

a common-mode sense circuit (e.g., **206**) connected to the first and second output nodes and adapted to generate a sensed common-mode voltage signal (e.g., **208**);

a differential amplifier (e.g., **207**) connected to receive the sensed common-mode voltage signal and a desired common mode voltage signal (e.g., Vcmref) and adapted to generate and apply a common-mode error-correction signal to the first and second inductance-creating elements to correct for differences between the sensed and the desired common-mode voltage signals;

a first variable capacitor (e.g., CL1) connected between the first output node and a second reference voltage; and

a second variable capacitor (e.g., CL2) connected between the second output node and the second reference voltage such that the circuitry is adapted to provide a continuous-time filter (CTF) function, wherein:

the first differential transistor pair comprises transistor M6 and transistor M7;

the first load device comprises transistor M4;

the second load device comprises transistor M5;

the first inductance-creating element comprises transistor M2;

the second inductance-creating element comprises transistor M3;

the power-supply rejection element comprises transistor M1 and current source I1;

a first input node VIP is connected to the gates of transistors M6 and M9;

a second input node VIN is connected to the gates of transistors M7 and M8;

the sources of transistors M6 and M7 are connected to the first current sink;

the drain of transistor M6 is connected to the first output node VON and to the source of transistor M4;

the drain of transistor M7 is connected to the second output node VON and to the source of transistor M5;

the drains of transistors M4 and M5 are connected to the first reference voltage VDD;

the gate of transistor M4 is connected to the drain of transistor M2;

the gate of transistor M5 is connected to the drain of transistor M3;

the sources of transistors M1, M2, and M3 are connected together and to receive the common-mode error-correction signal; and

the gates of transistors M1, M2, and M3 and the drain of transistor M1 are connected together and to receive the current from current source I1.

18. The invention of claim 17, wherein the current of current source I1 is controlled by a control signal that is adapted to be adjusted to adjust equivalent resistance provided by transistors M2 and M3.